

ABSTRACT

A sampling clock generation circuit and a data transfer control device make it possible to ensure a set-up time and the like during sampling, while maintaining a high frequency. A sampling clock generation circuit comprises an edge detection circuit detecting between which two edges an edge of data DIN (data to be transferred in USB 2.0 HS mode) is located, the two edges are among edges of clocks CLK0 to CLK4 that have the same frequency but mutually different phases, and a clock selection circuit, which selects one of CLK0 to CLK4 based on this edge detection information and outputs the thus-selected clock as a sampling clock SCLK. When the set-up time of a D flip-flop of the edge detection circuit is T_S , the hold time is T_H , and the period of the clock is T , N which is the number of a multi-phase clock is given by: $N \leq [T/(T_S + T_H)]$ (where $[X]$ is the maximum integer that does not exceed X). The clock that has an edge that is shifted by a set number M from an edge of the data DIN is selected as SCLK.